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March 16, 2008

Kurt Kessel
NASA TEERM Principal Center

Testing Printed Rework Traces – PWB Inc. Job Number E08_0088

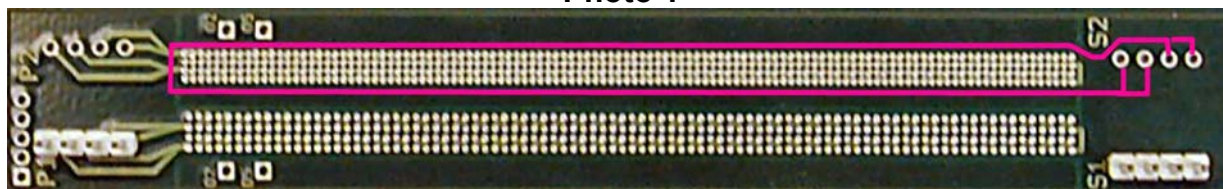
Twelve Interconnect Stress Testing (IST) coupons with a “printed trace” applied on layer one were received by PWB Interconnect Solutions and subjected to incoming inspection and prescreening.

The coupons had test traces printed on the solder mask using an advanced metal deposition method. The deposition or prototyping technologies used for creating printable electronics emerged from a Defense Advanced Research Projects Agency (DARPA) program titled Mesoscale Integrated Conformal Electronics (MICE). The program ran from 1998 through 2003 and developed a number of advanced direct write technologies. The Center for Accelerated Applications at the Nanoscale (CAAN) at the South Dakota School of Mines and Radiance Technologies are working to further refine the technologies for DoD applications. The method, mesoscopic integrated electronics conformal deposition, uses a silver based ink, to create a conductive trace. The trace was applied directly on the solder mask as indicated in Photo 1. After application the coupon was subjected to a low temperature thermal at 170°C to cure the ink.

The coupons were IST design GT32400. This design is an integrated coupon with IST test patterns on two grids; .032” and .040”. The .032” grid, test circuits P1 and S1, were used in this evaluation.

The scope of this test was to evaluate the reliability of a unique rework procedure where a conductive trace was printed on the surface of the coupon. The goal was to evaluate if this procedure could be used as a possible rework to substitute missing wirebonds for TSOP-50 components that will be used to evaluate board level interconnects for the NASA-DoD Lead-Free Electronics Project study of lead free assembly.

Approximation Location of Printed Trace **Photo 1**





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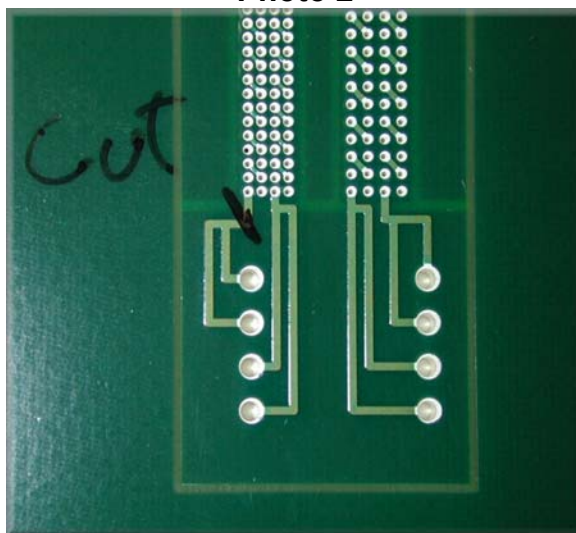
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In order to isolate the test circuit S2 for this evaluation, a cut was made on the back of the coupon. The cut effectively isolated the S2 circuit allowing the resistance to be measured exclusively of the printed trace. The printed trace resistance was measured to be ~9.4 ohms using a four wire ohm meter.

IST Coupon Modification for Measuring and Testing

Photo 2





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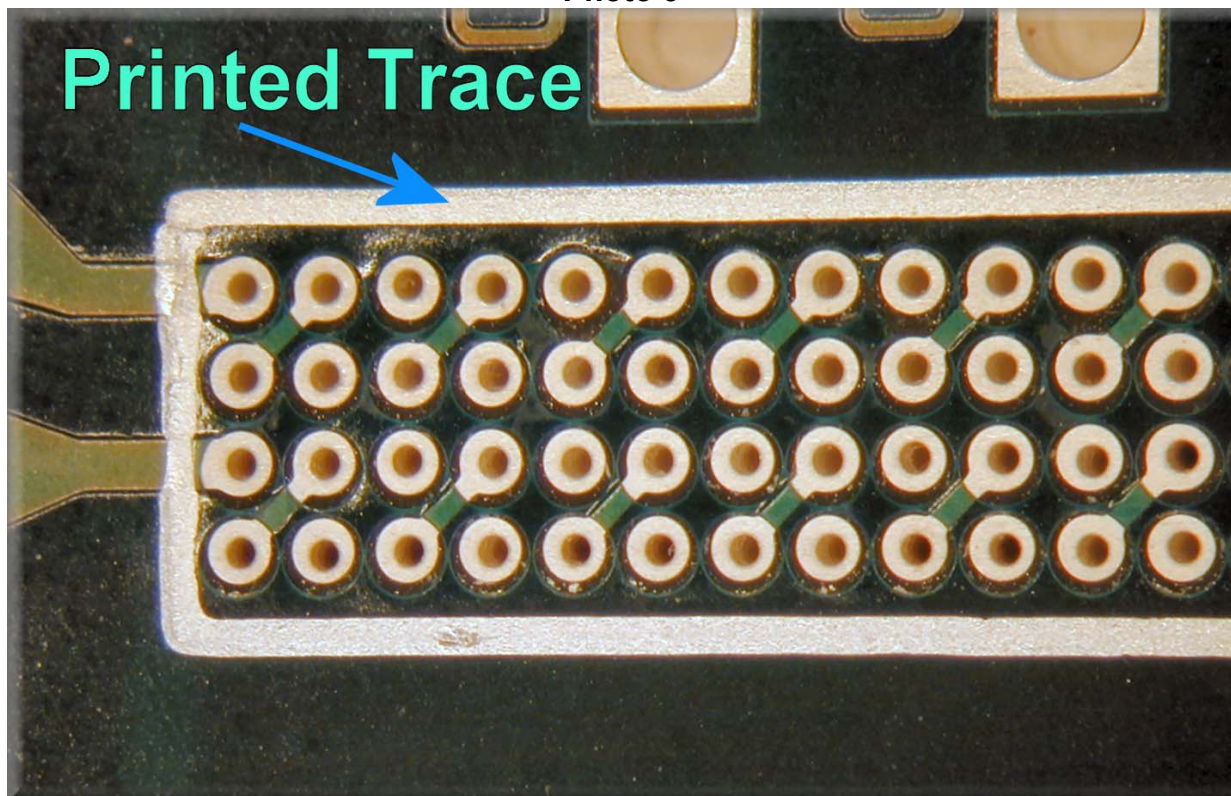
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A macroscopic evaluation revealed a conductive trace was printed on the surface of the solder mask. The line definition was not as well defined as a "print and etch" conductor, but it was considerably better defined than most "nomenclature" inks used for identification on circuit boards.

Printed Trace Around .032" Grid PTHs
Photo 3





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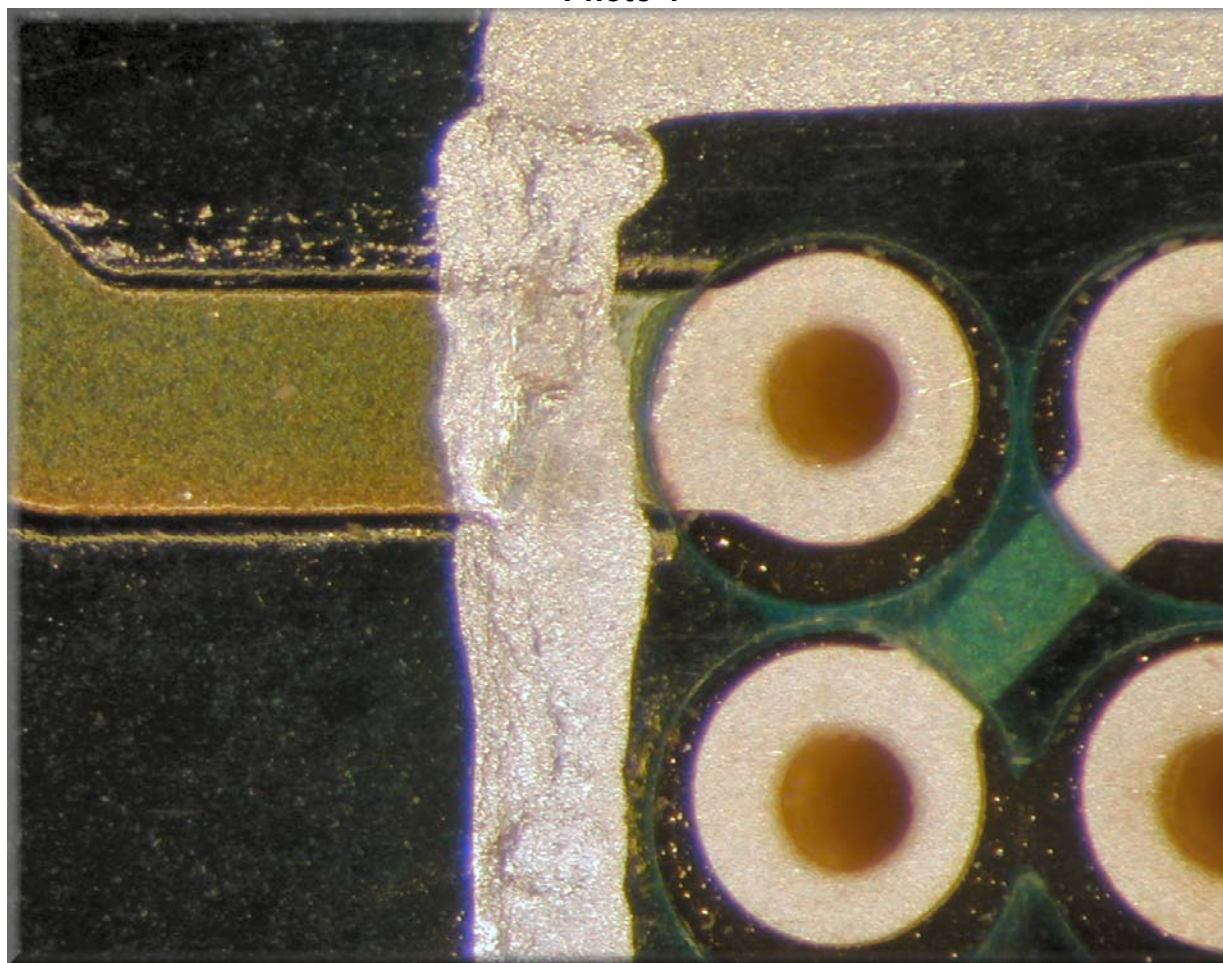
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The “conductive ink” was able to accommodate the “bumps” associated with copper traces under the mask. There was a change in the width of the trace to accommodate the varying topography of the PWB.

Printed Trace over Copper Conductors **Photo 4**





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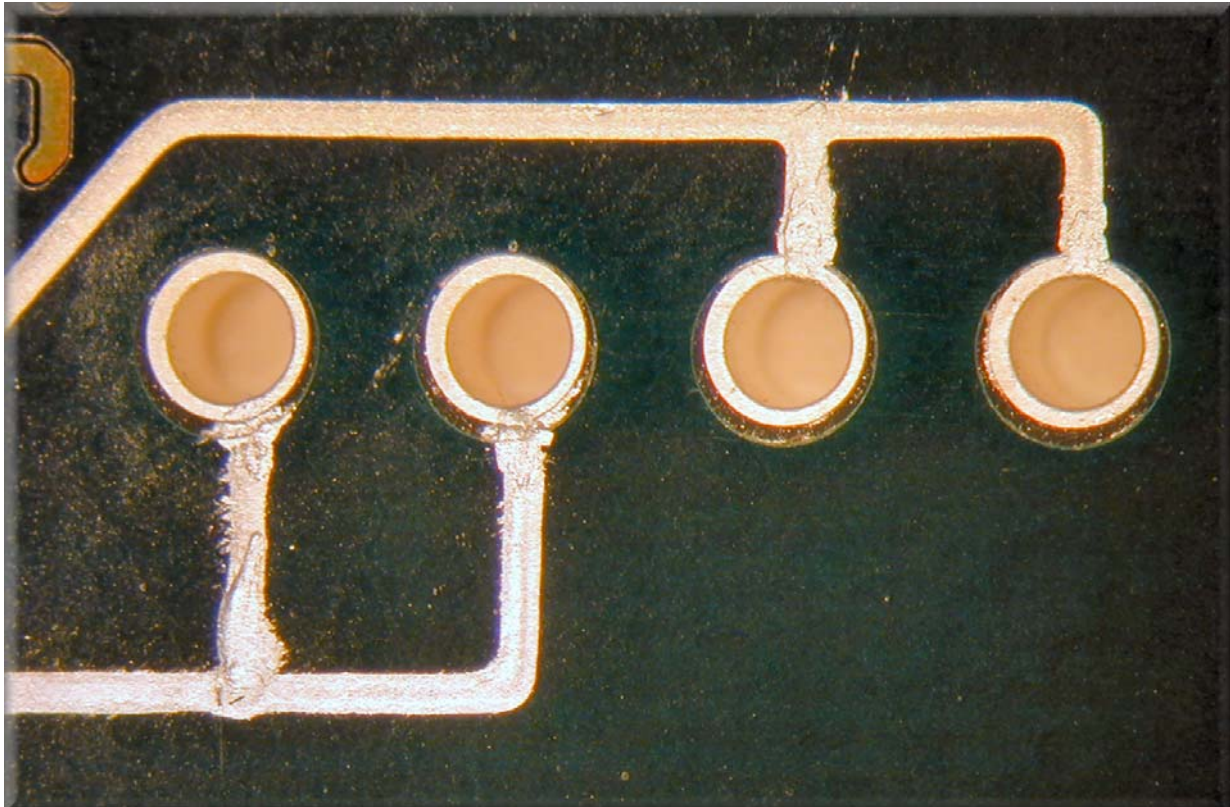
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The greatest challenge would be to print a conductive trace between the solder mask and an adjacent plated through hole. The topography requires the ink to produce a continuous path across the surface of the solder mask, down the side wall of the solder mask, across the exposed base material, up the wall of the PTH pad and into the hole. It would be naive to think that an ink, even though viscous, would not demonstrate some degree of bleeding in that application. Macroscopic examination did demonstrate some bleeding in the space between the solder mask clearance and the pad of the PTH. There was no indication that this condition was detrimental to the coupon. Some degree of bleeding should be expected and be taken into consideration in the end use application.

Printed Trace at PTH Pad
Photo 5





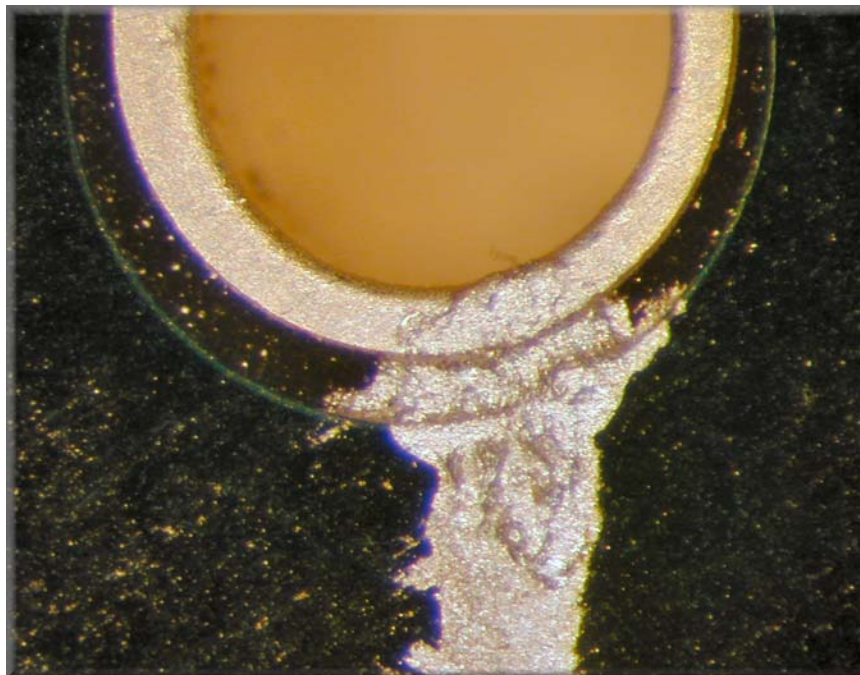
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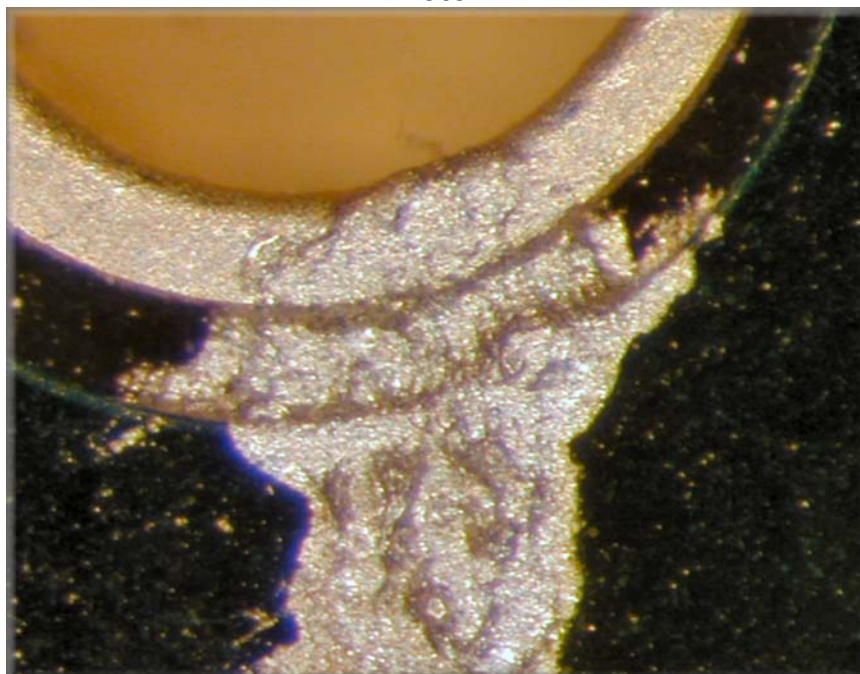
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Printed Trace at PTH Pad
Photo 6



Printed Trace at PTH Pad
Photo 7





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IST Testing is performed by heating the coupon internally with the power circuit while sensing changes in resistance in the “sense” circuit. In this case the sense circuit is the printed trace and the heating circuit is the power circuit P2.

In order to test the integrity of the printed trace using the IST method the resistance had to be reduced to less than 4 ohms. A connector was soldered into the plated through holes and a one ohm shunt was added to bring the sense circuit resistance into a testable range for IST equipment. This rework would allow testing but at a cost of not being able to stop testing immediately when a 10% increase in resistance on the printed trace was achieved. With this configuration the IST tester becomes an event detector that would be sensitive to an open in the printed trace.

Coupon 63 with Connector

Photo 7

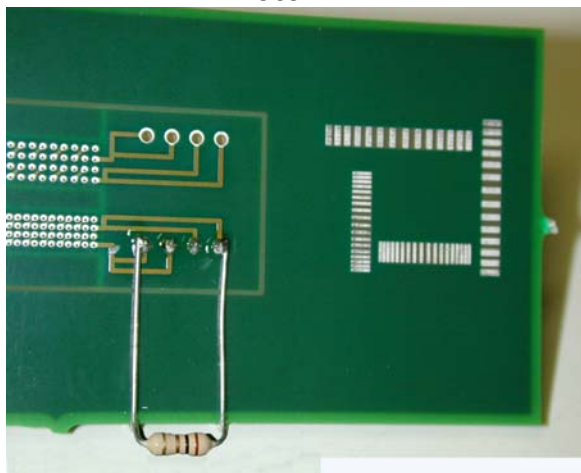
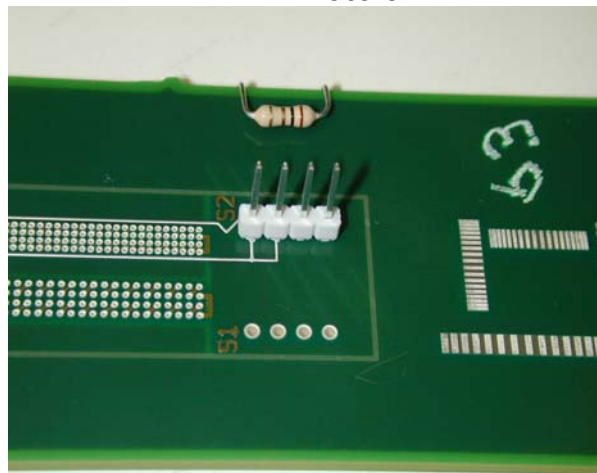


Photo 8



Coupon 63 was modified as described above and heated to 260°C three times to simulate lead-free assembly then subjected to thermal excursions to 150°C. The test was set to run 500 cycles. The printed trace survived lead-free assembly simulation (3X260°C) and achieved 500 cycles without failure.

Three coupons modified to accommodate IST testing were cycled to 260°C for 100 cycles to simulate multiple assembly and rework cycles to lead-free temperatures. This “survivability” testing allowed us the shortest test time to failure. The IST coupons tested at 260°C achieved a mean of 59 cycles before failure. The failures, however, were on the power circuit used to heat the coupons. The printed trace showed no evidence of failure or damage accumulation for the duration of the test. It could be inferred that the printed traces are more robust than the internal copper traces in this application.



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Respectfully submitted,

Paul Reid

A handwritten signature in purple ink that reads "Paul Reid". The signature is written in a cursive, flowing style.

Program Coordinator
PWB Inc.